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HIGH-SPEED ENERGY-EFFICIENT LOW-LEVEL VOLTAGE LEVEL CONVERTERS WITH STACKED MOS TRANSISTORS FOR LOW-POWER APPLICATIONS.

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ABSTRACT:

Optimization of power consumption in any System on Chip is one of the most essential requirements for applications like wireless sensor networks. Voltage level converters perform this conversion while interfacing the devices with various voltage domains. With buffers, Level Up converters can be implemented without any overhead. This research proposes buffer architecture to realize Voltage Level Converter. The proposed Voltage Level Converter uses an effective Transmission Gate, Positive Metal Oxide Field Effect Transistor, and Negative Metal Oxide Field Effect Transistor to improve the efficiency of the Level Voltage Converter. The performance of the proposed LC architecture is verified by implementing it in the Spectre circuit simulator. The proposed architecture, while implemented on 90nm CMOS Technology, gives the result of voltage conversion from 650 mV, 570 mV, and 540 mV to 1.85 V by the architectures. Architecture has an improved propagation delay of 36 %, 34 %, and 38 % to the Basic Level Converter. Thus, the proposed architecture is Timetime-efficient and energy-efficient.

Keywords: Transmission Gate, Positive Metal Oxide Field Effect Transistor, Buffer, Energy-efficient, Time Efficient, Level Converter.

1. Introduction

Low power consumption, low area occupancy, and high speed are the most essential requirements of any System on Chip application. Different methods have been published to improve the system's power efficiency on Chips and portable devices. Voltage scaling is one of the solutions proposed to improve the power efficiency [1, 2]. However, voltage scaling may degrade the device's performance because of the propagation delay. Dynamic supply voltage instead of Voltage Scaling can compensate for this degradation. In this technique, the most significant and critical parts of the time sensitivity of any device are supplied with the required voltage level, and the parts with lower time sensitivity for the functionality of the devices are provided with scale-downed voltage [3]. The use of a dynamic or multi-voltage supply can lead to a situation where low-voltage parts drive the higher-voltage parts of the device, which results in a leakage current [4]. Leakage current contributes to the static power dissipation at the MOSFET structure's reverse-biased PN junction diode [5, 6, 7]. Dynamic power dissipation occurs because of capacitance's charging and discharging processes at load. Therefore, scaling and structuring load capacitance is essential to minimize dynamic power consumption.

Voltage level converters are used to realize this different supply voltage level for the other parts of the same device. The most crucial function of any Voltage Level Converter is to

convert the voltage levels [8]. Level Converters can be Level Up or Level Down converters. Voltage Level Converters can also connect the device and I/O Circuitry [9,10]. Voltage Level Converters can optimize power consumption by giving structural variations [11, 12].

2. BASIC LEVEL CONVERTERS

2.1 Cascaded Inverters

A basic level converter can be constructed with the cascaded inverters [13]. Schematic of the commonly used Basic Level Converter is illustrated in Figure 1. The source of the PMOS transistor of the First inverter is supplied at a high Voltage level. The gate of PMOS and NMOS of the first CMOS Inverter is coupled to the input, which determines the output of the first inverter. For the high-to-low transition of the input signal, P1 gets switched on, whereas N1 gets switched off. Because of P1, High supply voltage is connected to the output of the first inverter, which in turn drives the second inverter.

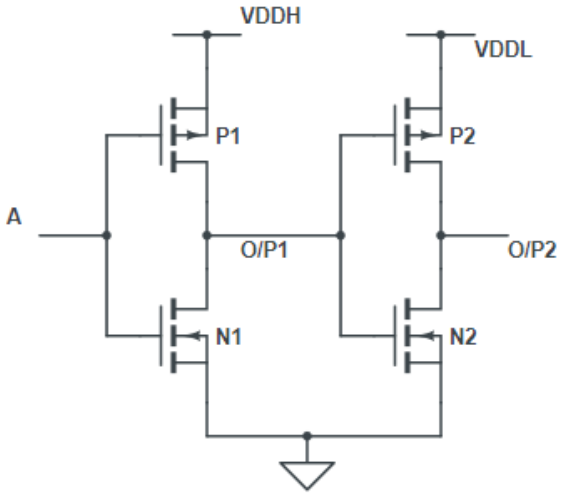

Figure 1: Basic Level Converters

In other words, the output of the first inverter acts as an input signal to the second inverter. The source of P2 is connected to the low supply voltage. O/P1 is high; it switches off P2 and Switches on N2. Thus, it connects the output of the second inverter with the ground. For low to high transition, P1 gets switched off, whereas N1 gets switched on. Therefore, the output of the first inverter is at ground level. O/P1 switches on P2 and Switches off N2. Thus, it connects the output of the second inverter with the supply voltage. The main drawback of this structure is the large amount of shoot-out current leakage when both PMOS and NMOS are open simultaneously. Besides this, thick oxide transistors must be used to withstand the high supply voltage. The usage of thick oxide transistors leads to more significant area consumption.

2.2 Cross-Coupled Voltage Level Converter

The schematic structure of a cross-coupled voltage level converter is shown in the figure. The output of the third inverter is connected to the gate of the PMOS of the second inverter, and the output of the second inverter is connected to the gate of the PMOS of the third inverter. The Gate of N2 is connected to the input signal, and the gate of N3 is connected to the output

of the first inverter. The gate of both transistors P1 and N1 are associated with the input. The second and third inverters are connected to the high voltage supply, whereas the first inverter is supplied with a low voltage. P1 switches off, and N1 switches on for low to high transition. O/P1 gets discharged to ground level. N2 gets turned on because of the input signal. Which also causes the O/P2 to be discharged to ground level. O/P2 switches on P3 and causes O/P3 to get charged to a high voltage level.

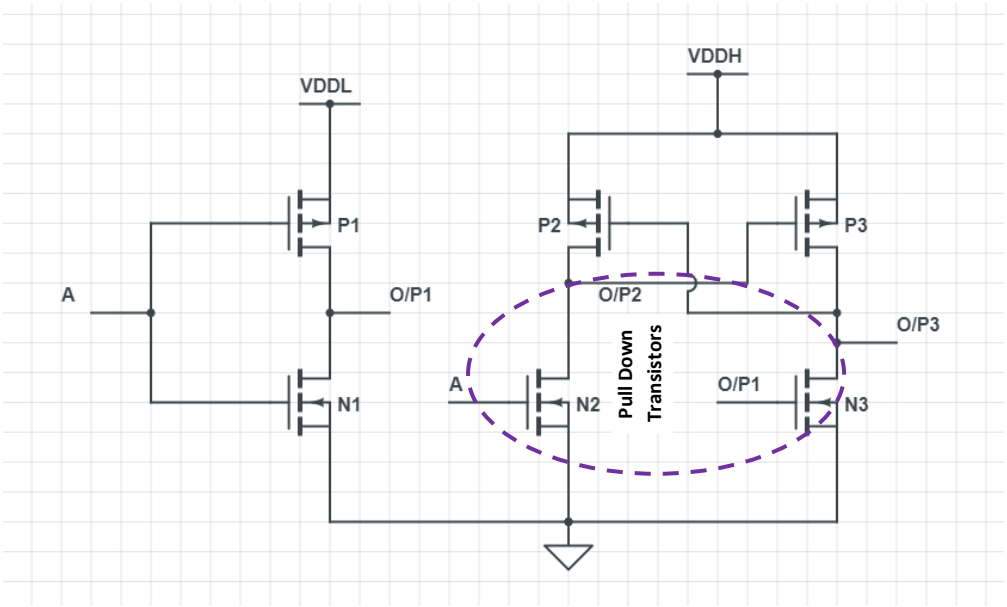

Figure 2: Cross-Coupled Voltage Converter

For high to low transition, P1 switches on, and N1 switches off. Because of this input signal, O/P1 gets charged to the low-level supply voltage. O/P1 switches off N2 and switches on N3. O/P3 gets discharged to ground level, thus making P2 a closed circuit. O/P2 gets charged to a high supply voltage level because of P2. The pull-down device weakens and cannot draw the output node O/P2 to the ground appropriately when the input voltage approaches lower levels. Because of this, the discharge time of the output node takes longer. Thick oxide layer transistors can be used instead of thin transistors for both pull-up and pull-down transistors. The only shortcoming with the Cross cross-coupled voltage level Converter is to withstand high supply voltage. Thick oxide transistors are essential.

3. TRANSMISSION GATE BASED VOLTAGE LEVEL CONVERTER

The Schematic of the proposed Level converter that uses Transmission Gate to improve its efficiency has six transistors. Four transistors function as buffer circuits, and the remaining two transistors form the transmission gate.

Transistors P1 and N1 are connected to perform as an inverter, and the output of the first inverter is connected to the input of the second inverter formed by P2 and N2. The source of the P1 is connected to the Transmission Gate such that the voltage drop across the Transmission Gate acts as the supply voltage to the first inverter. The supply voltage of the Transmission gate and second inverter is connected to Vdd.

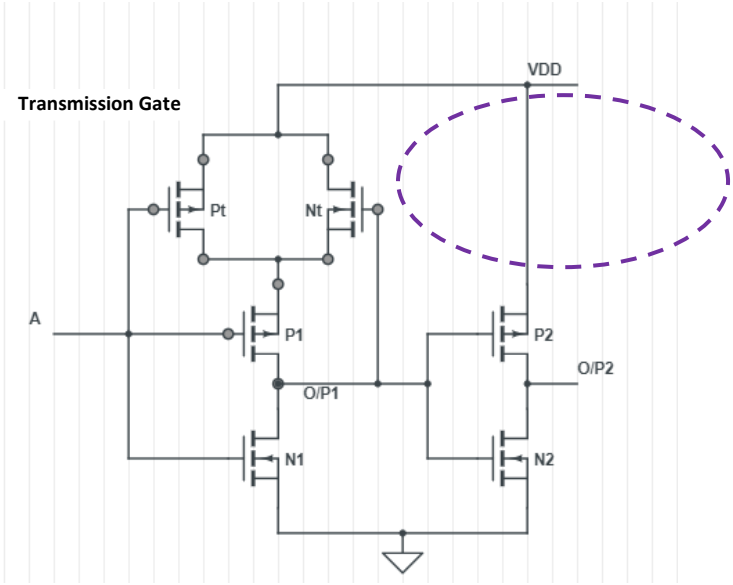

Figure 3: Transmission Gate based Voltage Level Converter

Transistors Pt and Nt act as a Transmission Gate that transmits the input to output whenever the signal at the gate is active. The gate of the transistor Pt is connected to the input of the buffer, whereas the input of Nt is connected to the output of the first inverter.
The proposed architecture is analyzed for switching conditions from high to low and low to high voltage levels. First, Pt and P1 transistors are turned on for high to low-level voltage transition where N1 turns off. Because of P1, the output of the first inverter gets to Vdd through the Pt transistor of the Transmission Gate. Additionally, during the transition from high to low, the first inverter's output turns the transistor Nt on. Production of the first inverter gets charged to Vdd quickly because of this additional path from Vdd to O/P1. O/P1 acts as an input signal to the second inverter. When O/P1 gets charged to Vdd, it switches on N2, establishing a connection between the ground and O/P2. Thus, the output of the second inverter discharges quickly to the ground or 0 V. Also, Nt is directly connected to Vdd through the Transmission Gate structure, so quick discharge is possible for high-to-low transition.

For low to high transition, Nt in the transmission state gets turned if O/P1 is at Vdd, thus connecting Vdd to the P1 transistor. But P1 is turned off, therefore making an open circuit between Vdd and O/P1. But N1 gets turned on, thus establishing a connection between O/P1 and ground. Thus, O/P1 will be at ground level or at 0V. After O/P1 gets to 0 V, Nt is turned off, avoiding the connection between Vdd and the first inverter. When O/P1 is at 0 V, N2 gets turned, and P2 gets turned. Because of this condition, O/P2 gets charged to Vdd through the P2 transistor.
Because of the arrangement of Nt and Pt transistors, there is a low resistance path between Vdd and P1 since one of the transistors is always on. It may cause leakage current to a considerable amount.

Suppose the gate of Pt is connected with the ground instead of the input signal. In that case, it always establishes a connection between Vdd and P1, which cancels the effect of utilizing the Transmission Gate Structure. It can be compensated by increasing the wire length between Vdd and P1. Since wire resistance comes to the rescue by having some voltage drop at P1.

4. PMOS-BASED VOLTAGE LEVEL CONVERTER

The Schematic of this new structure has a PMOS transistor stacked one above the other instead of a transmission gate in the Transmission gate-based Voltage Level Converter. The path from Vdd to P1 gets established if the gates of Pt1 and Pt2 are maintained at 0 V. Performance analysis of this PMOS-based Voltage Level Converter is analyzed for both transition levels, high to low and vice-versa.

The input signal is connected to the gatesP1, P2, P3, and N1 gate. Meanwhile, the output of the first inverter is connected to gate terminals of P4 and N2. The source of P1 is associated with Vdd, and the drain of P1 is attached to the source of P2. The source terminal of PMOS P3 is connected to the drain terminal of P2.

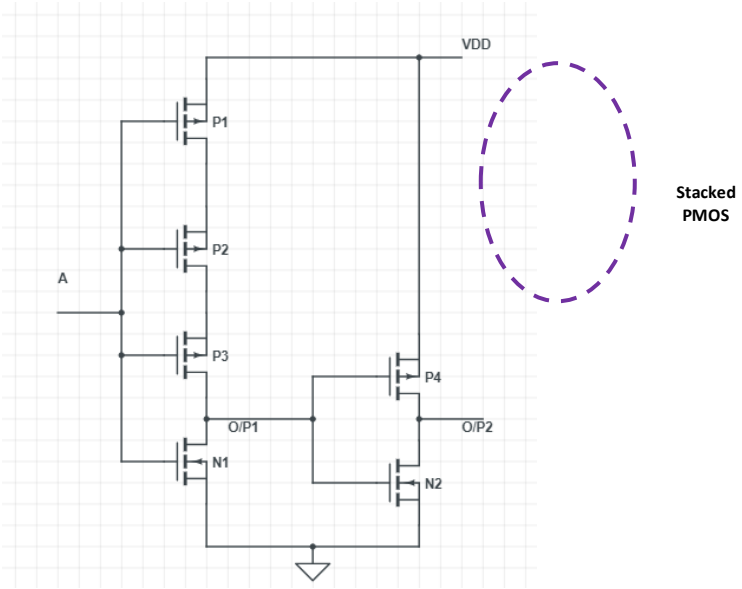

Figure 4: PMOS-based Voltage Level Converter

For high to low transition in the input signal, P1 and P2 get turned on and establish a path between Vdd and P3. At a low level, input P1 also gets switched on, thus charging the O/P1 to Vdd. Then, O/P1 makes N2 turn on after reaching the threshold voltage of N2, and P4 gets turned off because of the O/P1 voltage level. Because of this, O/P2 gets connected to the ground and discharges quickly.

For low to high transition at the gate of P1 and P2, both P1 and P2 remain off, providing high resistance between Vdd and P3, whereas N1 gets turned on, thus allowing O/P1 at 0 V. Because of this O/P1 level, P4 gets turned on, and O/P2 gets charged to Vdd.

The relationship between the input signal voltage and the voltage drop across the source of P3 is given in the figure. These two structures reduce the voltage drop across the first inverter considerably compared to the Basic Level Converter. From the results, it is clear that the transmission-based Level Converter has a voltage drop of 0.54 V at 1.34 V. In contrast, the based Voltage Level Converter has a voltage drop of 0.56 V at 1.45 V. From this, it is clear that the based Voltage Level Converter has a higher voltage drop compared with the transmission-based Level Converter. Therefore, the PMOS-based Voltage Level Converter is power efficient. Even when there is a delay in the rise time of the buffer, power consumption is reduced significantly. Due to the lesser voltage drop across the source of P3, it helps switch off the P3 and switch on N1 at a slightly faster rate. Thus, O/P1 gets discharged to 0V and, in turn, switches on P4. Therefore, the voltage level was made from O/P2 to Vdd.

5. NMOS BASED VOLTAGE LEVEL CONVERTER

The schematic arrangement of the transistors to realize an adequate Level Converter is shown in the figure. Here, NMOS transistors are additionally stacked up with the pull-up transistor of the first inverter. The input signal is directly connected to the gate terminal of P1, N1, and N3. Vdd is connected to a source of P1, P2, and N2. The source of N1 and N2 are connected to the ground, whereas the gate terminal of N2 and the source of N3 are connected to O/P1. The gate of P2 is connected to Vx, the voltage drop at the junction of N3 and N2. The gate of N2 is connected to O/P1, and the output obtained at the second inverter is denoted as O/P2.

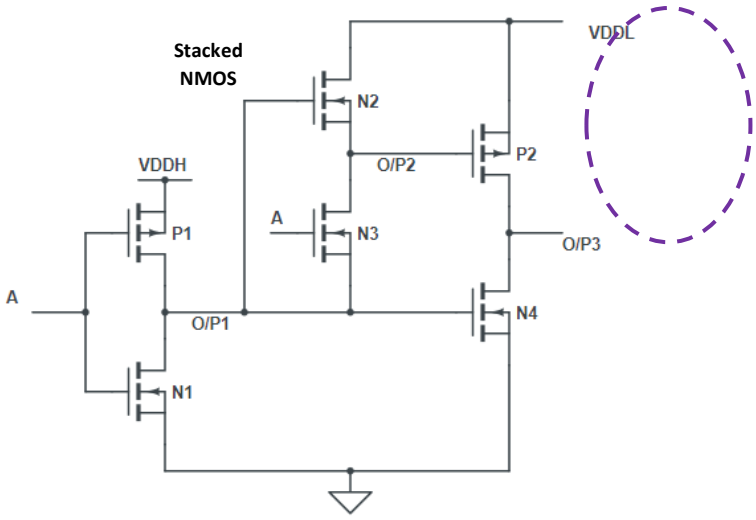

Figure 5: NMOS-based Voltage Level Converter

For low to high transition, P1 is switched off, while N1 and N3 get switched on, resulting in the Voltage level at O/P reaching ground level. Since N3 gets turned on, it establishes a connection between O/P1 and the gate of P2. Because of O/P1 and N2, N2 gets switched off, and P2 gets switched on, resulting in Vdd at the O/P2.

For high to low transition, N1 and N3 are switched off while P1 gets switched on, resulting in Vdd at O/P1. Because of this voltage charge, N3 gets turned off, and N2 gets turned on. The gate of P2 gets connected to Vdd, which turns off P2. Because of Vdd at O/P1, N2 gets turned on, allowing O/P2 to be discharged to ground level.

The NMOS-based power consumption is significantly reduced because the NMOS and PMOS transistor arrangement eliminates the shoot-through current. Also, the switching speed of the NMOS is higher than that of PMOS since, in general, the mobility of electrons is always more significant than the mobility of holes. NMOS occupies a lesser area than PMOS. So, the NMOS-based Level Converter is more efficient than the Transmission gate-based Level Converter and PMOS-based Level Converter.

Switching activity in all the types of buffer remains the same. Thus, the rise and fall time remains the same for all the level converters discussed in the above sections.

6. EXPERIMENTAL RESULTS

6.1 Simulation

The proposed Level Converter is implemented in 90 nm CMOS Technology, and functional verification is done using Spectre. The obtained results are compared with the Basic Level Converter and Stacked Dual Step Level Converter for the effectiveness of the proposed

architecture. The input signal considered for the simulation has a rise/fall time of 5 ns, and the voltage level ranges from 0.8 V to 1.8 V. For comparative purposes, the existing Basic Level Converter and Stacked Dual Step Level Converter stacked PMOS Level Converter are also simulated in 90 nm CMOS Technology, and the results are compared. Figs. 6 and 7 show the propagation delay and power dissipation as a function of supply voltage VDD.

From Fig 6, it is observed that a coupled Level Converter takes a much longer Time to give the required conversion when compared with other level converters. A stacked NMOS Level converter is efficient in terms of the total Time consumed for the voltage conversion. Transmission gate LC is faster than that of PMOS LC but less fast than NMOS LC. This is because NMOS LC exhibits a faster High to Low transition than other types of LC. From Fig 6, it is clear that for all the LCs, the propagation delay gets reduced as the VDD increases. Fig 7 shows the static power consumption of the level converters when the supply voltage is increased from 600 mV to 1 V.

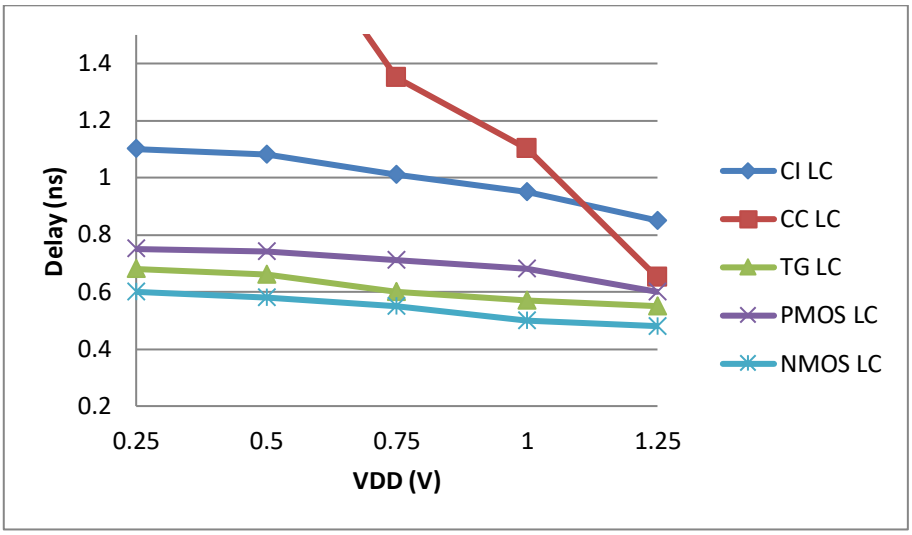

Figure 6: Simulated result analysis of Propagation delay of Level Converters as a function of VDD

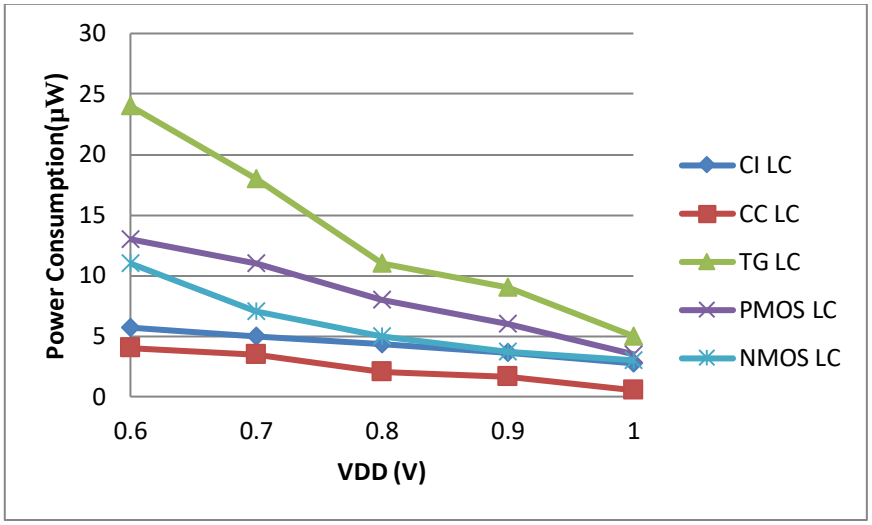

Figure 7: Simulated result analysis of Power consumption of Level Converters as a function of VDD

Power dissipation of a level converter decreases as the supply voltage increases. From Fig 7, the Transmission gate LC consumes more power than all other LCs because of the high static

power consumption. Cross-coupled LC shows better performance in power consumption than that of the proposed LC. NMOS LC is moderate in power consumption as it consumes 11µW and 3µW at 600 mv and 1 V, respectively.

6.2 Implementation Results:

Table 1 gives a comparative analysis of the resources required by the different designs of level converters implemented in 90 nm CMOS Technology. For analysis of the performance of the level converters, Area, propagation delay, total power consumption and voltage drop, rise time, and fall time are considered in this research.

Table 1: Analysis of resource utilization for Level Converters in 90 nm CMOS Technology

Parameters	Stacked Dual Step Level Converter [15]	Basic Level Converter [14]	Transmission Gate-based Level Converter	PMOS-based Level Converter	NMOS-based Level Converter
Power Consumption(W)	12.33	5.21	8.90	7.36	7.54
Propagation delay (ns)	7.63	11.93	7.62	7.89	7.36
Area (μm^2)	0.52	0.636	0.636	0.636	0.594
Rise Time (ns)	21.35	21.83	21.42	21.68	21.53
Fall Time (ns)	7.42	19.32	7.31	7.68	7.42
Voltage Drop	0.62	0.73	0.65	0.57	0.54

From the experimental results, PMOS-based LC consumes 7.36 nW during its entire functionality, which is 17 % and 2.4 % less power than Transmission Gate-based LC and NMOS-based LC. All these three LC architectures are suitable for converting lower input voltage levels. Basic LC is efficient for low-power applications since it consumes significantly little power compared to other LCs.

While analyzing the architectures for the delay performance, it is evident that transmission-based LC takes 7.62 ns whereas PMOS-based LC takes 7.89 ns, Stacked Dual Step LC takes 7.63 ns, and NMOS-based LC takes 7.36 ns to deliver the output. On comparing the four-level Converters, Basic LC has the worst performance in propagation delay. Basic LC's low to high transition delay is very high. NMOS-based LC has better performance in terms of the LC's operational speed compared to LCs.

On analyzing the Area required to implement the LC, NMOS-based LC required 0.594 μm^2 while PMOS and Transmission gate-based LC required 0.636 μm^2 and Stacked Dual Step LC required only 0.52 μm^2. Stacked dual-step LC has less propagation delay and less area requirement than PMOS and transmission gate-based LCs. However, the power consumption for the voltage level conversion is very high for stacked dual-step LC.

Table 2: Analysis of resource utilization for Level Converters in 0.18µm CMOS Technology

Parameters	Stacked Dual Step Level Converter [15]	Basic Level Converter [14]	Transmission Gate-based Level Converter	PMOS-based Level Converter	NMOS-based Level Converter
Power Consumption	11.38	6.18	8.83	8.08	7.97

(W)					
Propagation delay (ns)	6.34	6.87	6.48	6.07	5.87
Area (μm^2)	0.517	0.607	0.6037	0.597	0.604
Rise Time (ns)	19.38	20.456	21.734	22.36	22.843
Fall Time (ns)	6.93	18.4	7.865	7.343	7.86
Voltage Drop	0.53	0.67	0.59	0.534	0.537

Resource utilization of the Level Converters is implemented in 0.18µm CMOS Technology, and the results are listed in Table 2.

The transient response of the proposed Level Converter is given in Figure 8. From Figure 8, it is clear that voltage level 3.3 V is given as input, and our Stacked NMOS Level Converter converts the input voltage into 5 V. Thus, voltage conversion in a wide range is possible through Stacked NMOS LC.

Therefore, our proposed architectures are suitable for high-speed applications requiring power efficiency as their priority over area efficiency and lower voltage level conversions. Stacked Dual Step LCs can be implemented for applications that require area efficiency

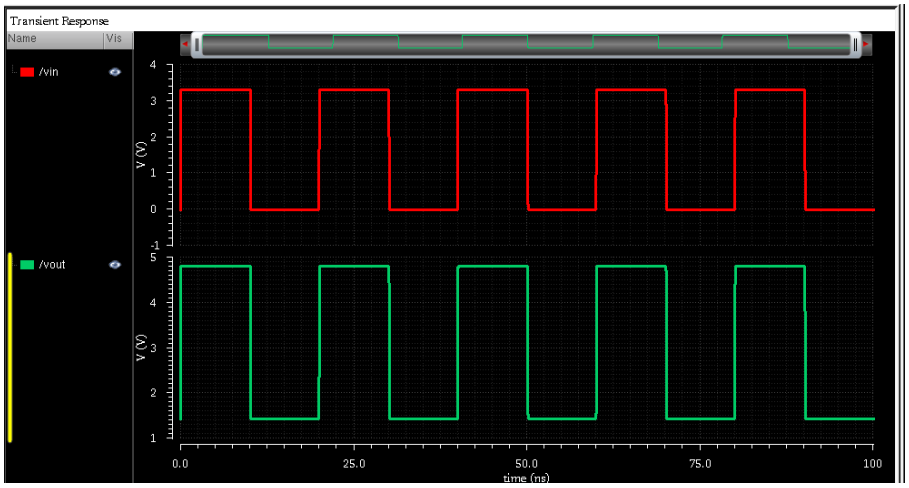

Figure 8: Waveform of proposed Stacked NMOS LC converting 3.3 V to 5 V at 1 kHz

7. CONCLUSION

This research article proposes three power-efficient and high-speed Voltage Level Converters with Transmission Gates, PMOS, and NMOS structures. Modified buffer structures are efficient in terms of propagation delay and power consumption. Among the three proposed architectures, NMOS-based LC is more Time- and power-effective than the others. Implementation in 90 nm & 0.18 µm CMOS Technologies also suggests the same theoretical observations. The implementation result indicates that the proposed techniques suit low-power and high-speed applications.

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