https://doi.org/ 10.33472/AFJBS.6.5.2024. 7894-7902





Validation of PCB design for ABS product in automotive industry. Smriti Sinha¹ A Asuntha², Raheem Basha³

1. Department of Electronics and Control Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamil Nadu

2. Department of Electronics and Instrumentation Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamil Nadu 3.Continental Automotive India³

e-mail: asunthaa@srmist.edu.in

Article History Volume 6, Issue 5, 2024 Received: 22 May 2024 Accepted: 29 May 2024 doi: 10.33472/AFJBS.6.5.2024. 7894-7902 **Abstract** — This paper investigates a meticulous approach to validate Printed Circuit Board (PCB) designs specifically tailored for Anti-lock Braking System (ABS) products within the automotive sector. The primary focus is on the application of Design for Manufacturability (DFM) and Design for Assembly (DFA) principles to optimize the reliability, manufacturability, and efficiency of ABS PCBs. The paper presents detailed analyses, case studies, and practical insights into integrating DFM and DFA in ABS PCB design and validation processes.

Keywords—: DFM, DFA, PCB CAM tool, PCB, ABS, Validation techniques, Immersion tin.

I. INTRODUCTION

The Anti-lock Braking System (ABS) plays a pivotal role in the dynamic landscape of automobile safety, mitigating risks associated with sudden braking. Central to this technology is a sophisticated network of Printed Circuit Boards (PCBs) orchestrating the ABS system's operation. Given the perpetual evolution in car engineering, ensuring the reliability and optimal functionality of PCB designs is paramount. This study explores the realm of PCB design validation for ABS products, with a specific emphasis on enhancing the effectiveness of these crucial components by integrating Design for Manufacturability (DFM) and Design for Assembly (DFA) concepts.

The automotive industry is witnessing a paradigm shift towards advanced safety features, necessitating a corresponding evolution in underlying technologies. ABS systems, designed to prevent wheel lock-up during braking, epitomize this progress. The seamless coordination of multiple components is essential for ABS functionality, with PCBs acting as the central nervous system orchestrating intricate signals and controls. The efficacy of ABS relies heavily on the dependability of its constituent PCBs, necessitating a robust validation procedure that surpasses standard practices.

A foundational aspect of this research lies in Design for Manufacturability (DFM), recognizing the inherent interconnection between designs and manufacturing processes. DFM principles guide the PCB design process, optimizing it for productive and economical manufacture. Ensuring alignment with manufacturing capabilities, DFM reduces the likelihood of errors and expedites the production process. Within the ABS domain, where precision is paramount, DFM becomes an indispensable facilitator for achieving maximum production efficiency while upholding product quality. This encompasses considerations from component location to signal integrity, temperature management, and material selections.

Concurrently, Design for Assembly (DFA) principles contribute to the efficiency of the subsequent assembly process. Given the integration of a diverse array of electronic components in ABS products, the ease with which these components come together during assembly is crucial. DFA principles guide design to enhance manufacturability, simplify assembly procedures, and decrease the probability of errors during assembly.

The research integrates DFM and DFA principles into the validation process, aiming to enhance the reliability and performance of ABS products' PCB designs. Through a comprehensive analysis and systematic validation approach, the study seeks to offer valuable insights to the automotive engineering community, fostering advancements in ABS technology. Consequently, this research aspires to be at the forefront of shaping the future of ABS technology through meticulous PCB design validation, contributing to the ongoing evolution of automotive safety standards and enhancing the overall safety and performance of modern vehicles.

Design for Manufacturability (DFM) in ABS PCBs:

- Defines key principles of DFM and their relevance to ABS PCB design.
- Explores strategies for optimizing ABS PCB layouts to streamline the manufacturing process.
- Discusses material selection, component placement, and routing considerations to enhance manufacturability.

Design for Assembly (DFA) in ABS PCBs:

- Introduces DFA principles and their significance in ABS PCB design.
- Analyzes strategies for simplifying assembly processes and reducing production time.
- Examines the integration of automated assembly techniques to enhance the overall efficiency of ABS PCB manufacturing.

Benefits and Impact:

- Quantifies the benefits of incorporating DFM and DFA in ABS PCB design.
- Analyzes the impact on manufacturing costs, reliability, and time-to-market.
- Presents a comparative analysis of ABS PCBs designed with and without DFM and DFA principles.

Validation Techniques for DFM and DFA in ABS PCBs:

- Provides an overview of simulation tools and methodologies for validating DFM considerations.
- Describes testing protocols to verify the effectiveness of DFA strategies in ABS PCB assembly.
- Discusses the integration of prototyping in the validation process to ensure real-world applicability.

II. LITERATURE SURVEY

Xiaoxiao Song, Keyu Wang, Zhuo Chen, Kaixu Ren, Peng Liu. The impact of four typical surface finishes on electrochemical migration in printed circuit board production was studied using a modified water drop test, and the electrochemical migration phenomena of each surface finish at different bias voltages were analyzed. Based on the analysis of the experimental results, the four surface finishes were ranked in terms of their ability to resist electrochemical migration, as follows: electroless nickel/immersion gold (ENIG) > lead-free hot air solder leveling (HASL) > HASL > Cu. In the PCB manufacturing industry, metallic surface finishing of the exposed electrodes on the PCB is critical for improving reliability, conductivity, and solderability. The sensitivity of different PCB electrode surface finishes to ECM (Electrochemical Machining) varies widely. Several studies have been conducted to analyze the ECM phenomenon with common metallic materials on PCBs, including pure tin,[2][8] tin- based solder alloys,[1][9][10] and sintered nano- silver.[11][12] Similarly, some of the studies were based on different surface finishes of PCBs, including hot air solder leveling (HASL),[13] immersion silver (ImAg),[14][15] copper-clad laminate (Cu),[16] and electroless nickel/immersion gold (ENIG).[17][18].

III. METHODOLOGY

To validate the any design of the Printed Circuit Board it must gone through multiple stages. According to the customer need and specification, specification sheet is prepared which will contain all the requirements of the board like PCB Size, Base material, Base copper thickness of inner layer and the outer layer, Maximum Application temperature, Smallest / Largest hole diameter, requirement of press fit / single pin design, Minimum line width / minimum spacing laser drill vias (micro vias) requirement, Minimum Tg of base material, DSC (Differential Scanning Calorimetry), Thermal cycle requirement, capable for lead free profile in SMD, Copper surface finish like OSP (Organic Solderability Preservative) , HASL (Hot air solder leveling), Immersion silver, Immersion tin, ENIG (Electroless Nickel Immersion Gold), Closed hole requirement, Impedance, Carbon ink / silk screen, Fine pitch or BGA application, CAF (Conductive Anodic Filament) level and so on. Once project is awarded design of the PCB is ready to validate with the DFM and DFA. The file format should be open data base format so that tool is used to validate the design should be function properly. Analyzing the design according to the DFM & DFA guideline will prepare the deviation list which consist of blocking point during the manufacturing and hence send for the correction in the design.

Base material: The base material in PCB (Printed Circuit Board) serves as the foundation upon which the conductive traces and components are mounted. It provides mechanical support and electrical insulation for the circuitry and temperature resistance. Common base materials include FR-4: It consists of woven glass fabric impregnated with epoxy resin. FR- 4 offers excellent electrical insulation properties, good mechanical strength, and high temperature resistance, making it suitable for automotive applications like ABS systems)

Polyimide (PI): Polyimide prepregs, often referred to as "kapton," are known for their exceptional thermal stability and resistance to high temperatures. Polyimide materials can withstand temperatures well beyond those encountered in typical automotive environments, making them suitable for ABS PCBs operating in extreme conditions.

BT (Bismaleimide Triazine): BT resin-based prepregs offer high thermal stability, low dielectric constant, and excellent mechanical properties. These characteristics make BT prepregs suitable for high- frequency applications and environments with elevated temperatures, such as those found in automotive electronics.

Base copper thickness: It is the conductive material for routing electrical signal and power throughout of the PCB. Its value could be 35μ m, 70μ m, or 105μ m. The thickness value for outer and inner layer can be different or equal, depending on its requirement.

Smriti Sinha / Afr.J.Bio.Sc. 6(5) (2024). 7894-7902

Check for requirements like Leaser drill requirement: Requirement of microvias like Blind vias, buried vias; Thermal cycle requirement; Minimum line width and spacing requirement; Z-axis routed PCB; Minimum Tg of base material; TMA (Thermos mechanical Analysis); DSC (Differential Scanning Calorimetry).

Check points for analyzing the design before sending it for manufacturing.

Component outline to pad spacing: This is the clearance between the component pads to component outline. For manufacturing purpose this clearance should be the 300 µm according to IPC standard.

Component spacing: This is clearance between component outline to another component outline. And its minimum value should be 400µm according to IPC standard.

Component pad to pad spacing: This is the clearance between the component pad to another component pad and it should be 300 µm according to IPC standard

Component AOI: Component AOI (Automated Optical Inspection) spacing in PCB (Printed Circuit Board) manufacturing refers to the minimum distance required between components on the board to allow the AOI system to effectively inspect each component. This spacing ensures that the inspection equipment can accurately analyze and detect any defects or misalignments in the soldering, placement, or orientation of the components. The specific spacing requirements may vary depending on the capabilities of the AOI system and the size and type of components being used.

Copper in keep out area: This is the copper trace width which is connected to an IC pad shall not increase overall width of the pad.

Incorrect / missing mask clearance for SMD pad: It is the clearance between the SMD pads and solder mask. The minimum clearance is required 75 µm according to IPC standard.

Incorrect / missing mask clearance for PTH drill: It is the clearance between the PTH (Plated through hole) and solder mask. The minimum clearance is required 125 µm according to IPC standard.

Incorrect / missing mask clearance for NPTH drill: It is the clearance between the NPTH (Non Plated through hole) and solder mask. The minimum clearance is required 100 µm according to IPC standard.

Different net spacing: This the spacing error between two different potential.

Same net spacing: This the spacing error between same potential.

NPTH to Rout: This is the distance between the NPTH (Non plated through hole) and rout (copper). The minimum space requirement for outer layer (top and bottom) and Inner layer is different.

PTH to Rout: This is the distance between the (Plated through hole) PTH and rout (copper).

Drill stub: This is the non-connected drills in the board. Preferred to remove drill stub throughout the board.

Copper trace stub: These are the non-connected copper traces. Preferred to remove copper traces stub throughout the board.

Improvable routing: These are the copper traces with 90- degree bend which occupies more space in the board so preferred to give 45 degree of bending throughout the board.

PTH Annular ring: This is the surrounding copper around the plated through hole. This value different for inner and outer layer. It also depends on base copper thickness value of the board.

Copper on NPTH: It is preferred to no copper on NPTH (Non plated though hole).

Missing pad for PTH and vias: It is preferred to have copper pad for all the plated through hole and vias on the board.

Conductor width: This is the minimum value 0.1mm of the copper trace should be followed for good conductivity. And the clearance between the two trace is 0.13mm. These factors depend on the impedance value for the different layer of the board.

Incorrect drill to drill distance for plugged vias: This is the minimum distance between one centers of drill to another drill. Preferred to keep 0.4 mm. The closed vias need plugging.

Via plugging: Plugging is done only for the outer layer of the PCB. It is a process in which vias are filled completely with resin or closed with solder mask. This is different from via tenting where resin/solder mask doesn't fill the via hole but just provide a covering.



Missing drill: Drill must be provided for all through holes components.

Acute angle: Preferred to remove all the acute angle found in the board.



Fig: Acute angle in PCB

Coverage: It is the clearance between solder mask clearance and copper pad. The minimum clearance is required 0.075 it vary according to the design of the board like HDI (High density interconnect), Power board.

Thermal via: All power MOSFET or any microcontroller should not have via on pin as closed holes process. Even blind vias should not found on the pin.

Alignment of RC component: The component should be placed in zigzag patent to avoid mistake in AOI inspection.

Need split plane for solder paste layer: The splitting is required for solder paste layer to avoid the risk of soldering issue. There should be proper spacing between the solder paste to avoid heat dissipation.

Solder Paste related check: Check for paste missing area and small paste area throughout the board.

Missing thermal clearance: Thermal relief should be provided around all solder pad areas.

Restriction for selective soldering: Preferred to maintain 6mm clearance between SMD components outline to connector hole or any through holes component drill on soldering side for selective soldering. NPTH (Non plated through hole) should not be in selective soldering or dip soldering area.

Position of fiducial marking: It is a reference marks for proper recognition and positional alignment of the panel / PCB (Printed Circuit Board) in the solder paste printer, placement and other SMT machines.

DMC (Data matrix code) Marking: It is required for product traceability & PCB supplier traceability.

Tombstone error: A tombstone error in PCB (Printed Circuit Board) assembly occurs when one end of a surface- mounted component lifts off the board during soldering, resembling a tombstone. It results from unequal soldering forces or misalignment, causing electrical discontinuity and malfunctioning of the circuit.

It is required to maintain the trace ration of 300% to avoid tombstone effect in chip component for SMD soldering process.

Test point to test point distance: This the distance between one test point center to another test point center. Preferred to keep 2mm it may vary.

Test point to component distance: It is the spacing between test point to component outline should be as per component height.

Incorrect mask clearance for test point: It is the solder mask clearance for the test point. The minimum clearance should be 75 µm according to IPC standard.

Solder pastes on test point: Basically solder paste layer for test point is required only for OSP PCB surface finishing for good contact of nail.

Solder mask dam: A solder mask dam in PCB (Printed Circuit Board) manufacturing refers to a protective layer of material applied over copper traces to prevent unintentional solder bridges during assembly. It forms a barrier between adjacent solder pads, ensuring proper electrical isolation and preventing short circuits.

Preferred solder mask dam between pads 0.1mm. If needed, then solder mask clearance can be resized to maintain the solder dam 0.1mm.

BGA (Ball Grid Array) with component on opposite side: In double sided PCB (Printed Circuit Board) and in Multilayered PCB (Printed Circuit Board) if BGA (Ball Grid Array) is present then it is preferred to remove all the component from the opposite side of the BGA (Ball Grid Array). As BGA (Ball Grid Array) balls cannot be checked with X-ray inspection because 100% covered by another component.

Check point before Final package release for manufacturing.

Schematic DRC (Design Rule Check): To ensure that the design meets specific requirement regarding electrical, mechanical, and manufacturing consideration.

DRC (Design Rule Chesk) is important to list out the missing or any new component from the customer design. Schematic is required in BOM creation.



Parts Load: If any DRC error found the missing or new parts is Re-loaded in the library to get error free DRC.

Forward Annotation:

Load component position: All the components are load which is placed outside of the board design.

Saving component position: All the components are placed inside the board which is according to the customer design.

IDF Import:

Gerber import: Gerber file is created which consist of all the information related to routing in PCB (Printed Circuit Board). Whose output is called as Manufacturing package.

ODB (open data base) import: This ODB file is consist of X-Y Co-ordinated of the components. Which helps in creation of assembly drawing of the PCB (Printed Circuit Board).

Panel creation: Output Automation:

Design Check	Observation	Remar k
Copper in keep-out	5 7 IC 1500 10	Routing trace connected to an IC pin shall not increase the overall width of the pad.
Improvable routing	1 2 1	Preferer to avoid 90- degree routing from the board.
Copper on NPTH (non- plated through hole)		Preferred to remove unwanted copper from all NPTH throughout the board.
Drill to drill distance for all plugged/close d vias		Minimum distance between two drills should be 400 um.
Missing pad for PTH & via		Provide copper pad for all PTH & via throughout the board.
Incorrect mask clearance for tab MOSFET & center pad vias		Preferred to remove the solder mask on each open hole of the MOSFET tab center pad to permit the plugin adhesion
Need split plane for solder paste layer		Preferred to provide split plane for the solder paste layer to avoid the risk of soldering issue.
Thermal via error	0309	All power MOSFET should not have via on power pin as closed hole process
Alignments of RC component		
Restriction for selective soldering		Preferred to maintain 6mm clearance between the SMD component outline to



V. RESULTS

1	6	$\label{eq:rest} \begin{array}{c} \mbox{trend} & \mbox{trend} $	Ne Adria Niji * <mark>Eliteria</mark> Niji 2 Eliteria Agent 5 N	- Condense Tomate Standard Sta	The set of	ber * by O totat Fraits Bath Fraits Bath Select Temp
-		+ >	0 6 7 6 1		t	4
	Ē	ADDITIONAL QUESTIONS NOT CATAGORIZ	SE ABOVE	requirement (P : Proposal , R : Remark (D : Queries)	Customer feedback	Agreement
	×	Broar have	Risk description / Attachment			
		21 Copper in keep-out area :	ai	P: Rouling bases connected to an IC Pad shall not increase the overall with of the Pad. Please connect the errors	OK. Customer will connect read errors Update the genter files and connect information. Laycal to be ready by C- semptes production	
	•	27 Component spacing ACI :	πJ	P: Devise connect the attached error list in sequence wheel according to "given where of the rotate Distance tomouls: F2:1.5 x th ::	Rejected: Components cannot be stored: Sadeved joints shall be investigated by other methods (in g. ICT)	
		20 Paulphat Wanatah ;	러	P: Televise to brain the Contential statutures to trappets Contential and a list and the AP sign of the commis- tion of some year and ensist Contential to Copport paid through Statutures and Parko Contential Contential Annual Copport Paid Through Annual Annual Statutures and an Statut a statuture and annual contential contential and annual statutures and annual contential contential and annual to preferred a statuture and annual contential and annual to preferred a statuture and annual contential annual annual to preferred	Rejected contraver-uses the etanglard PEP per literary	
		24 Incomect mask clearance for GND Pad :	84	P. Pretmet Mask cleanare for INIC Pad as 11 an inversion according to Conferent agricultien. Pressor commit the entropy multiplication board Come 1. Can be connected by PCB Supplers Manufacture 1 Case 2. Hend to be connected by Castover: P. Inverse Law compared by Castover: P. Inverse Law compared to PTINs 100 km. Prese cannot the entropy	75 om maak claasieruw waa kept sollar maak openings ale defried by customer part threey	
		25 Wissing / Incornect mask clearance for PTH drill :	82	troughout the board Cose 1 - Can be corrected by PCB Suppliers Manufacturer 1	Fearlet	
	4	of Ortil Bub :	22	Case 2: Need to be controlled by Castomer P: Preferred to remove the chill Stub through out the board.	KADC and KTO are not populated OK, slidt will be removed	
	•	Component Check Issues : Example : 27 3 - Component outline to another component pad spacing 5 - Component spacing c. Dual forghmet issues	a2	P: It is difficult to check ALCorporate in indextremes in Call CARCord are to exits unity many Component a unifyringent readed the corporatif. Case 1: Reaso confirm the Components publishes with Confinential Guideleng pixes in adactment page. Case 3: Press Mody the COB Re., If exits maps of component card be connected.	Reported Costoner d'echedial clearances, which is IGNI dependent (there are excluding components, like LLTD and LGTT)	
		28 Terprovable routing :	21	 Performed to improve the routing (Error list is provided in attachment sheet). 	OK, errors will be corrected	
2	0 8 8 5 6	Component Check (Issues) : Component pairs . Component pairs to suither component pair spacing . Dual toopponent basies	až.	P: mis stifted to check. Al Componente Hollerd issues in Cost Chell bord due to bella stady mange ("component + a stady mange" anough the componente, Carden + Penere carden the Componente publiches with Controltat Cardenie genere instalt-ment page. Carden 1: Preses Under the COBE (et. et an ange al component cardine committed).	Rejected Calibrer: checked all ceaning es with its GOU dependent, these are escularing components, like UST1 and UST1	CLOSED-Kooped Componenti ale nati opcidadenthe sare the in natio
		normable routins :	500	P : Pretered to improve the routing (Error list is provided in attachment sheet)		0.0560
		Th Annahr Grag:	22	P : Uninnum simular mp to mare layer stock to Efform. Preside control the errors according to the Contentiat guidelines. FA : Units Association (Sociation et al. 1950) and R : Units Association (Sociatione) = 175pm 1950); Fer 2120; RA: Units Association (Sociatione) = 270pm R : Units Associatione) = 270pm R : Units Association (Sociatione) = 270pm R : Units Associatione) = 270pm R : Units Associatione) = 2	Gil, emps all be controlled	CLOSED Removed
	0 8	itoris (Open nats (Net Error) :	<u>113</u>	THE REAL PROPERTY OF THE PROPERTY OF THE REAL PROPE	Cannol confirm, since enors are not marked	den modication The comment combined in C scatter report
	, ,	Aning à H	McII	P - Pease provide the chill for the all Through hole components Need more detail on this point. Whether it has some internationally ?	K400 will not be populated, drifts will	CLOSED Accepted, sol poled, if it a starmy in the schematic For check approximation to remove it.
	2 0	Coverage / Exposed Copper / Incorrect Symbol:	86 ¹²	Remark : These are the losses with low impact to time (Genter modification can be done to species but Meed Distinger profession)	notibe provided OK, errors will be corrected when	DLOSED .
		are of sacing :	10-11	Remark : These are the issues with low inpact to true (Getter modification can be done by suppliers but Need Customer confirmation)	offerent nets are precised	01.0580 Reviewed during the meeting and appeal
			1	Remark : These are the issues with low impact to fine (Gerber modification can	OK, errors will be correctled	Cl. OSED. Reversed Compiler meeting and
	1	ave:	822 A	be done by suppliers but Need Clustoner confirmation (OK, errors all be corrected	agreed
	5 4	Alignment of RC component	1532 Y	r : reste toov ne connena saroaro guernes gies n assomen.	Reported. Componentis cannol be moved sostered joints shall be investigated by other methods (e.g. xCT)	Accepted that some posteries are that and to be respected in AOL and additional way to be respected meets to be validated (AOL) ICT (EOL Bestback is needed)
		1 1	0 1 1 6	 I I Prose maintain the 6 nm clearance between SHD components outline to 		Components in between connector pris
,	6 3	Restitutions for Beliective Boldering:	12.31	Corrector Anel any Yrings froe conquere et al is subleting and by benche soldering. (PTH visual for the in Secche Soldering of Dip Soldering ans	Clatamer resired guideline is 5.5 5 Gimm registed, lapool have by to Victobe the clamance as shuch as	obes not need required publicles. replanter the docks in that care to space muse in POD they can not be inicided an impaired care and an impection. (bottomapection also THT componets- actional Top wild is inspect care, to same oursets in other projects in service production. Electrical - Enclose list will be revealed Med provide Mediack to customer Top or wild dock 50 - Carepte
	, ,	Tombslace error :	<u>16-12</u>	P : It is required to maintain the trace ratio of 300% to avoid Tombalone effect Obji Components for SHD soldering Process . Pis correct the layout	 CK errors will be corrected in case chip size components (3005 or centaria) 	COST Available costster
		PCB Warking :	R28	P - Its required for product transability & PCB supplier traceability. Position & size can be continued after accurcing Process. Please continm .	Check 1007150_002 chapter 17	Position is DW, content to be continued by Position
		PTH & SPTH Tolerance :	1213	P : PTH & NPTH preferred tolerance should be as per Continential Guidelines	Rejected, Keep the Castoner	Feedback is needed from POB suppler the can meet this pustomer oner
		Testpoint to Testpoint Distance :	163	P: spacing between One test point center to another test point center as 2 mm (Cost) standard value) through call the board. Please correct the erro accarding to the Continential guidelines.	6 Rejected curkaner publice is 20	to be reversed with plant that customer spec (2.00ml) is OK
		het replacement (27) :	<u>823</u>	Ament 1: Need connecter COB File to the detailed analysis of free point offer Fired point gaving and datases believes tend-part to other height composeds. To make at the subble for and in electring in CAM Tool the part area that method be used to COM File social to gave project and paragraphic method be used to COM File social to gave project and paragraphic method be used to COM File social to gave project and paragraphic Com File Research to Barling and Policies He below strap-dat. Com File Research to gave parameters be below strap-dat. Com File Research to Barling and Barling School Barling and School Barling Y	De Sojected Test point names and Subaron publications	Is reviewed with ICT in the plant if they can provide herefoart with this spec from costoner
	2	Selfer mask Dum :	R ₂	P. Henres Stater and Jacobeen Plans invasities of Malana. Proceedings of the Plans Proceeding of the Plans Proceeding of the Plans Plan	Bolder mask openings and dams a defined by XB part labors. Unterland dams to 155 um by KB-padelines	3) be invested with plant if soliter mask dar Call to achieve in items of advancedly to be checked by construer possibly to advanced to be advanced to the soliter mask being Stould with soliter mask opening for IC pasts control FGB proce invesses is not needed.
ĺ	Ţ	8.1.1.0.7.1.	100	P : Pease follow the Continential standard guidelines given in attachment.		CLOSED. Reviewed during the needing and agreed

Figure 2: Feedback report from customer



06	net ki tet ki Apro +][[×.∉.k]	e si ka	de :	5 30 X	Calls	tetraj Anaya Sendhely Wadawar
4 4	8 C	0 E F 0		- E - E - E - E - E - E - E - E - E - E	τ	1
58 34 57 SI. NO	Others (If any) ADDITIONAL QUESTIONS NOT CATADORIZED		e Rating	regiment (P)Proposit (R:Renati (Q)Queries (Customer feedback	Agreement
52 Q1	Copper in keep-out area :	H2	4	P: Rouling Taxes connected to an IC Pad shall not no rease the overall with of the Pad. Please correct the errori.	CK. Dustance will carrect real errors Update the patient lies and correct information. Layout to be ready by C- samples conduction	CLOSED. Reviewed during the modify and agreed
60	Conguriert spusing ACI :	<u>82</u>	Y	P: Pease const the allocked once liet in respective sheel according to "given easier" of the Tasie. Dataset formula: 12:11.8 M	Rejected Components canvalitie moved Soldered patts shall be revestigated by other methods (e.g. (CT)	Accepted that some positions are not able to be inspected in 4/0, and addited way to be inspected means to be validated. (ACV/ICT / EOL feedback is needed)
Q5	Poolprint microsofth :	n3		P: Proteined to takina the Continential standard budgenets Continential Prad Takit Baspe of Soliter Prad - Instrangie with 40° scipe in the corrers Baspe of Soliter parts and Patic Desamon from Cogney paid P: Shape of Soliter Takin - Housepaid to Cogne Apentine Experie Housepair and Prade Desamon Standard Area Takit as below - Strebust Taking American Convents Standard Area Takit as below	Rejected customer uses the standard KD part Ricray	CLOBED, Revealed during the meeting and agreed
4	Incorrect mask clearance for SMD Pad:	H		Professional basic conserves for 5000mg as 37 services an excerting the Destroyed parameters of the service of the excertision of the comparation because Date 1: Cancel connected by 925 Supplem/Annatocker ? Date 2: Next to be connected by Costoner	75 um masik clearance was kept policie mask operangs are defined by calaterer cale from	Feedback oppected from undranker Q4 sing T420 was converting, well of them also Neutrien wide or head-tempers.
as	Missing / Incorrect musik clearance for PTH dnill :	R2		P: Perlened Wark cearance for PTHis 100 un. "Rease correctifie errors broughout the board Case 1. Can be corrected by PCB Supplers/Manufackuer 7. Case 2. Need to be corrected by Dastoner	Regestrati X425 and X12 are not populated	Accepted, it is during in the scherballs.
05	Dril Ibo:	at .		P: Petered is remore the did blat through out the board.		



Fig: Output file for Manufacturing

VI. CONCLUSION

In summary, the incorporation of DFM and DFA principles into the PCB design validation process for ABS products is pivotal in achieving a balance between design complexity, manufacturability, and assembly efficiency. This approach not only ensures the production of high-quality electronic products but also contributes to cost savings, shorter time- to-market, and increased overall customer satisfaction. As technology continues to evolve, the importance of DFM and DFA in PCB design validation remains paramount for the success of electronic products in the competitive market landscape.

VII. REFERENCES

- 1. B.K. Liao, H. Wang, S. Wan, W.P. Xiao, and X.P. Guo, Electrochemical migration inhibition of tin by disodium hydrogen phosphate in water drop test. *Metals* 10, 12 (2020).
- 2. K. Piotrowska, M. Grzelak, and R. Ambat, No- Clean solder flux chemistry and temperature effects on humidity-related reliability of electronics Journal of Electronic Materials. 48, 1207 (2019).
- 3. M.S. Jellesen, D. Minzari, U. Rathinavelu, P. Moller, and R. Ambat, Corrosion failure due to flux residues in an electronic add-on device. *Eng. Fail. Anal.* 17, 1263 (2010).
- 4. K. Dusek, D. Busek, P. Vesely, M. Placek, T. Reichl, and J. Sedlacek, Analysis of a failure in a molded package caused by electrochemical migration. Engineering Failure Analysis 121, 105 (2021).
- 5. H. Conseil-Gudla, F. Li, and R. Ambat, Reflow residues on printed circuit board assemblies and interaction with humidity. *IEEE Transactions on* Device and Materials Reliability 21, 594 (2021).
- 6. X. Zhong, In situ study of the electrochemical migration of tin in the presence of H₂S. Journal of Materials Science: Materials in Electronics 31, 8996 (2020).
- E.L. Lee, A. Haseeb, W.J. Basirun, Y.H. Wong, M.F.M. Sabri, and B.Y. Low, In-situ study of electrochemical migration of tin in the presence of bromide ion. Scientific Reports 11, 15 (2021).
- 8. S.Y. Jiang, B.K. Liao, Z.Y. Chen, and X.P. Guo, Investigation of electrochemical migration of tin and tin-based lead-

free solder alloys under chloride-containing thin electrolyte layers International Journal of Electrochemical Science 13, 9942 (2018).

- O.N. Kamil, O.F. Rifdi, and A.F. Che, Electrochemical migration and corrosion behaviours of SAC305 reinforced by NiO, Fe₂O₃, TiO₂ nanoparticles in NaCl solution. IOP Conference Series: Materials Science and Engineering 701, 012 (2019).
- B.K. Liao, H. Wang, L. Kang, S. Wan, X.D. Quan, and X.K. Zhong, Electrochemical migration behavior of lowtemperature-sintered Ag nanoparticle paste using water-drop method. Journal of Materials Science: Materials in Electronics 32, 5680 (2021).
- 11. G.Q. Lu, C.Y. Yan, Y.H. Mei, and X. Li, Dependence of electrochemical migration of sintered nanosilver on chloride. Materials Chemistry and Physics 151, 18 (2015).
- 12. M.S. Hong, and J.G. Kim, Method for mitigating electrochemical migration on printed circuit boards. Journal of Electronic Materials 48, 5012 (2019).
- H.L. Huang, X.M. Guo, F.R. Bu, and G.L. Huang, Corrosion behavior of immersion silver printed circuit board copper under a thin electrolyte layer. Engineering Failure Analysis 117, 14 (2020).
- P. Yi, K. Xiao, C.F. Dong, S.W. Zou, and X.G. Li, Effects of mould on electrochemical migration behaviour of immersion silver finished printed circuit board. Bioelectrochemistry 119, 203 (2017).
- 15. K. Xiao, P. Yi, C.F. Dong, S.W. Zou, and X.G. Li, Role of mold in electrochemical migration of copper-clad laminate and electroless nickel/immersion gold printed circuit boards. Materials Letters. 210, 283 (2018).
- 16. P. Yi, K. Xiao, K.K. Ding, C.F. Dong, and X.G. Li, Electrochemical migration behavior of copper- clad laminate and electroless nickel/immersion gold printed circuit boards under thin electrolyte layers. Materials 10, 137 (2018).
- 17. X.F. He, M.H. Azarian, and M.G. Pecht, Evaluation of electrochemical migration on printed circuit boards with lead-free and tin-lead solder. Journal of Electronic Materials. 40, 1921 (2011).
- B.I. Noh, J.W. Yoon, W.S. Hong, and S.B. Jung, Evaluation of electrochemical migration on flexible printed circuit boards with different surface finishes. Journal of Electronic Materials 38, 902 (2019).
- 19. W.S. Hong, and C. Oh, Lifetime prediction of electrochemical ion migration with various surface finishes of printed circuit boards. Journal of Electronic Materials 49, 48 (2020).
- D. Bušek, K. Dušek, J. Kulhavý. Dendritic growth and its dependence on various conditions. 2018 41st International Spring Seminar on Electronics Technology (ISSE). 1 (2018).