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# HIGH SPEED INDUCTORLESS DC-DC CONVERTER FOR ENERGY HARVESTING APPLICATION

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**Abstract:** The need of less power, area systematized and high speed converter for energy harvesting application is pushing to design this fully integrated inductor less Dc-Dc converter. This architecture is designed to boost very low voltage to the supply voltage used for the implantable low power electronics. Starting from the 300mV input voltage, the converter reaches up to more than 1.2V regulated output voltage and providing output current up to 5µA without any external excitations. Power management is taken care by regulation circuit. The major aim of this project is to examine, design and simulate an inductor less Dc-Dc converter using cadence virtuoso tool in 45nm technology. The converter must keep the output voltage constant when the input voltage changes. And also compared with the previous work in terms of technology, startup circuit, Input and Output voltage and with the Efficiency.

**Keywords**: *charge pump, regulation, latched comparator, energy harvesting.*

## INTRODUCTION

**T**he size of the electronics devices has been gradually reducing after the establishment of integrated circuits (chips). While designing any chips, designer has to take care of the parameters like power consumption, speed and the chip area. The CMOS technology is widely used for constructing these kinds of integrated circuits, as CMOS technology provides low power consumption and smaller area [1].. The low power electronics is one of the best design methodologies for power saving and power management. To power the wearable and implantable less power electronic circuits such as intraocular pressure or active contact lenses requires an exceedingly small factor. Because, these low power electronics doesn't tolerate any surface mounting components or the standard batteries due to the minimal size for implant ability. As a result, energy harvesting becomes a very favourable alternative to achieve battery replacement [2].

Energy Harvesting is a scientific process in which a small factor of energy captured by the environment, that would be in the form of light, heat, sound, vibration and wind, is transformed into an electrical energy or into a useful form of energy. The photovoltaic (PV) energy or light energy naturally exists in the environment (0.1Mw/cm2 ~100mW/cm$^2$). By using thin film photovoltaic cell, photodiodes or solar cells, the photovoltaic energy harvesting is done in which light energy is converted in to electrical energy. Their output voltage levels are very small (300mV~ 5oomV) and also depends on the light intensities [3]. This low voltage is justiciable for the digital operations, but it is very low and less

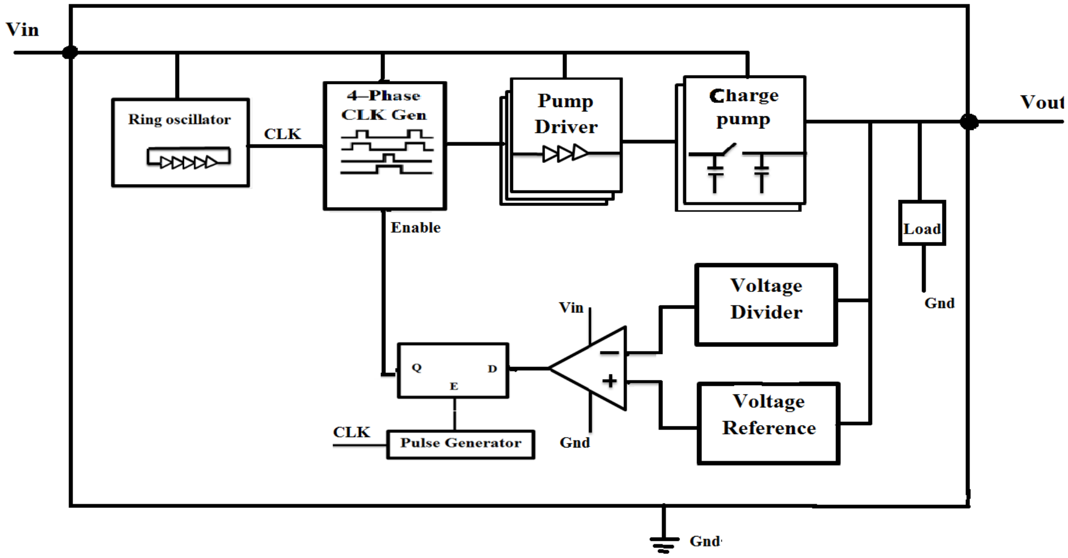

**Fig.1:** Block diagram of the inductor less DC-DC converter IC.

Stable compared to the Supply voltage required for the Analog sub-sections of the IC. The IC's required at least 1V of stable voltage. Therefore, one intermediate low power IC is required to provide a regulated Dc-Dc voltage from the energy harvesting system. Analog device offers this kind of low power IC's for Energy Harvesting applications.

In this project, we proposed a fully-integrated low power Dc-Dc converter for implantable sensor using Energy Harvesting. In this work a regulated step up converters are used to give regulated voltage from the unregulated low voltage obtained by the PV energy harvesting. Simultaneously the converter steps-down the current as the result of the energy conservation principle. Due to the area constraint, an inductor-less Dc-Dc converter is used. Because of miniaturized system we cannot use any external start up voltage. The main objective of this work is to work with less voltage without any external excitation for the regulated DC voltage of more than 1V under different conditions of light. The proposed work exhibits a start-up voltage of 300mV to achieve regulated voltage of 1.2V. This work is preferred for the high efficiency, less input voltage and for small size.

## 1. PRIOR WORK

Photovoltaic is a method of converting light energy (solar radiation) into electrical energy. The Output voltage of the PV cells are very low, required a step-up converter to obtain Dc voltage input to the power electronics circuits. This converter must retain the constant output voltage when the Input voltage and the Output current changes. Inductor- based boost converter operate with the low input voltage and gives the high efficiency but required an off-chip inductor in the micro Henry range [4]. Due to the large area it is prohibited in certain applications where the size constraint is considered.

Thus the fully integrated capacitor charge pump converter is preferred. Compared to the inductor based converter, the charge pump converter consumes less area due to the absence of inductor. It was used for the battery recharging and it requires the high voltage battery for the star up. Later used switched capacitor pump to kick start the boost converter. It is not favorable to provide a startup voltage or the startup circuit to the low power electronic devices.

## 3. ARCHITECTURE AND CIRCUIT DESIGN

This design is a low power wireless sensing system integrated on a Biocompatible or an implantable intraocular device. Therefore the power and the size are the main constraints. The converter must be efficient and its size should be small. The Fig.1. Show the block diagram of the Converter IC.

### A. *Architecture*

The unregulated and un-boosted input voltages are used for powering the components of the IC except $V_{div}$ (Voltage divider) and the $V_{ref}$ (Voltage reference block). Four- phase clock generator derived from the clock generated by the ring oscillator. These are non- overlapping clocks and can drive 10fF capacitance. The converter used here is switched capacitor charge pump. Switching operation of the converter depends on the clock pulse. CP having large input impedance to drive this CP, the pump driver circuit is required. To boost the input voltage we use this forward path and to manage the power, regulation path is used. In the regulation path the boosted voltage is scaled down and compared with the reference voltage. If the scaled Output is lesser than the $V_{ref}$, the logic circuit enables the clock otherwise charge pump stops boosting.

### B. *Ring Oscillator*

The oscillatory behaviour is used in the circuit to turn on and turn off the circuit operation periodically. Most of the digital and electronic devices are shown this behaviour. Oscillators are used to generate oscillations depending up on their applications. Ring oscillator is one of the low power oscillators which consist of odd number of delay cells which are connected in series that means the output of present delay cell is given as input to the succeeding delay cell. The inverter delay cell consists of complementary pairs of PMOS and NMON transistors with symmetric parameters. The inverter gives low output when input is high and vice versa. Therefore PMOS called the Pull-Up and NMOS called the Pull-Down network.

### C. *Four phase clock generator*

The system clock generated by oscillator cannot be used for the charge pump directly, but it is used to generate four clock

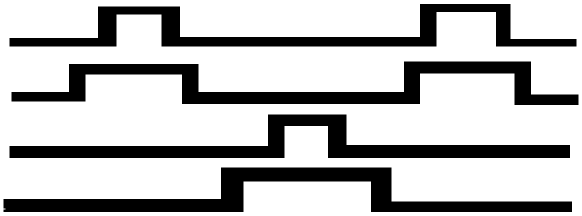

**Fig.2:** Four phase non-overlapping clock pulse.

phases, which are used for the charge pump. These four phase clocks are non-overlapping clock signals. The timing of switch transmission and the non-overlapping period depend on the clock generator. And the clock pulses are as shown in Fig.2. The generator circuit consists of logic gates, inverters and the buffer with different propagation delay [10]. This clock generator circuit is controlled by the regulation part.

### D. *Charge pump*

The Dickson charge pump is widely used for generating high voltage. This circuit is designed such that capacitors are inter-connected with diodes and coupled with non-overlapping clocks. We can use MOS transistors as diode by shorting the gate and drain terminals. The Diodes of the Dickson charge pump is changed by the N-MOS transistors as showing in figure Fig.3. To avoid the voltage drop across the transistors and reverse charge sharing phenomenon, the gate boosting concept is used. The four phase non-overlapping clocks are used for both gate boosting and also for charge pump application. The both Input voltage and the Clock amplitude should be same to power supply voltage ($V_{DD}$).

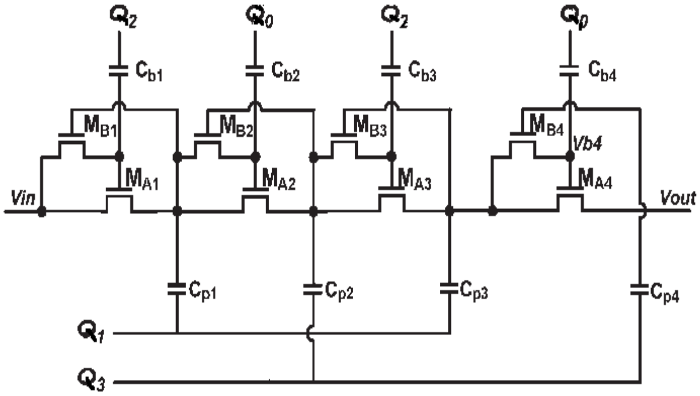

**Fig.3:** Block diagram of Four-stage Dickson charge pump

The Charge Pump cells are connected in cascade which ensures that the large voltage generated by each stage is fed to the next stage. The Output voltage of each stage is larger than the voltage generated from its previous state by the voltage of clock amplitude. To avoid the $V_{th}$ (threshold voltage) drop across transistors, gate boosting circuit is used which compensate the $V_{th}$ value to give $V_{gs}$ ~$V_{ds}$.

### E. *Pump driver*

When the CMOS integrated-circuit drives the big capacitive load leads to increase the power loss and circuit Delay in the chip. The effective way of reducing the power consumption of a circuit is to scale-down the supply voltage to reduce both leakage Energy and active energy. For some Applications such as implantable devices, Medical Instruments and Wireless Sensor Network where the reduction of supply-voltage is not possible, there the driver circuits are used to drive big distributed RC load by enhancing the switching speed and also used to reduce power consumption. These circuits reduce the dynamic Power Dissipation and limits voltage swing of the gate [13].

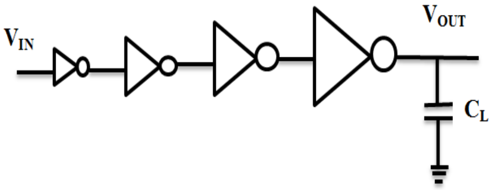

**Fig.4.** Block diagram of pump Driver circuits.

If the widen the transistor size by a scaling factor S, it would decrease the resistance value by S and increase the load capacitance by S to achieve low delay. Another driver circuit is required to drive this widen transistor. Thus the inverter chain is used. The Fig.4 represents the driver circuits. The inverters with gradually increasing size are connected back to back to drive large capacitance.

## F. *Reference generator*

Reference voltage generators are used in many applications such as A/D converters, D/A converters, flash memories and also used in communication systems. These circuits are having dependency on temperature in analog circuits. It affects the performance of the circuit. The BGR (Band Gap Reference) is in wide use to provide stable voltage reference in mixed signal CMOS signals. It is temperature, process and supply (should be greater than 1.2V) independent circuit, if these parameters varies also BGR produce constant output voltage. The output voltage of BGR is 1.25V which limits the BGR operation below 1.2V supply. CTAT and PTAT devices are used to make temperature independent and OPAMP or the current mirror circuits are used to make supply independent.

## G. *Latched comparator*

The conventional dynamic latched comparator architecture is used. Due to the regeneration latch, string positive feedback gives fast decision. The architecture of latched comparator is as shown in the Fig.5. The operation is as follows, when the clock is low, then $M_{tail}$ is off and $M_9$ & $M_{10}$ makes both the output nodes outp and outn to supply voltage ($V_{DD}$) and also called output reset transistors. Extra switching transistors $M_7$ and $M_8$ are added to improve the characteristics of the comparator, since those additional pmos transistors increases the time of the input transistors $M_1$, and $M_2$, are being operate in saturation when clock is high (during evaluation). When the clock is high, transistors $M_7$, $M_8$, $M_9$ and $M_{10}$ are OFF and $M_{tail}$ is ON. The input transistors start to pour with different rates proportional to the applied Input voltages from $V_{DD}$ to ground (zero). If $V_{ref} > V_{div}$, outp discharges faster than the outn, thus outp falls down to $V_{DD} - |V_{th}|$ before outn. The

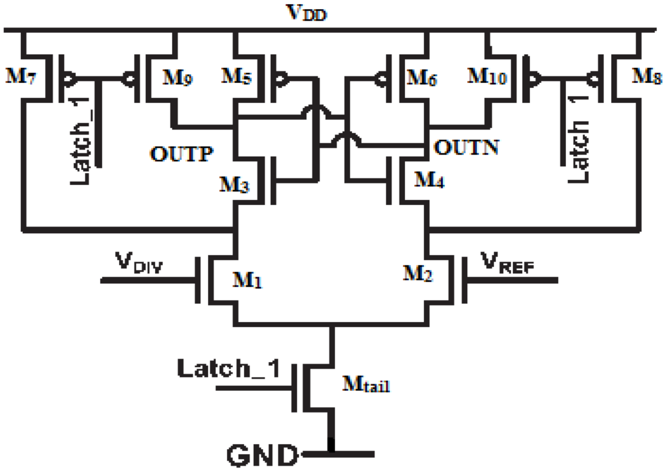

**Fig.5.** Block diagram of the latched comparator.

Corresponding P-mos transistor ($M_5$) gets turn ON which pull back the outn to $V_{DD}$, And vice versa [14].

## 4. RESULT

The integrated Inductor less Dc-Dc converter circuit module designed and simulated. If we give the input voltage to this module it will produce regulated DC voltage of 1.2V. The clock frequency is configured between 500 kHz to 1MHz.

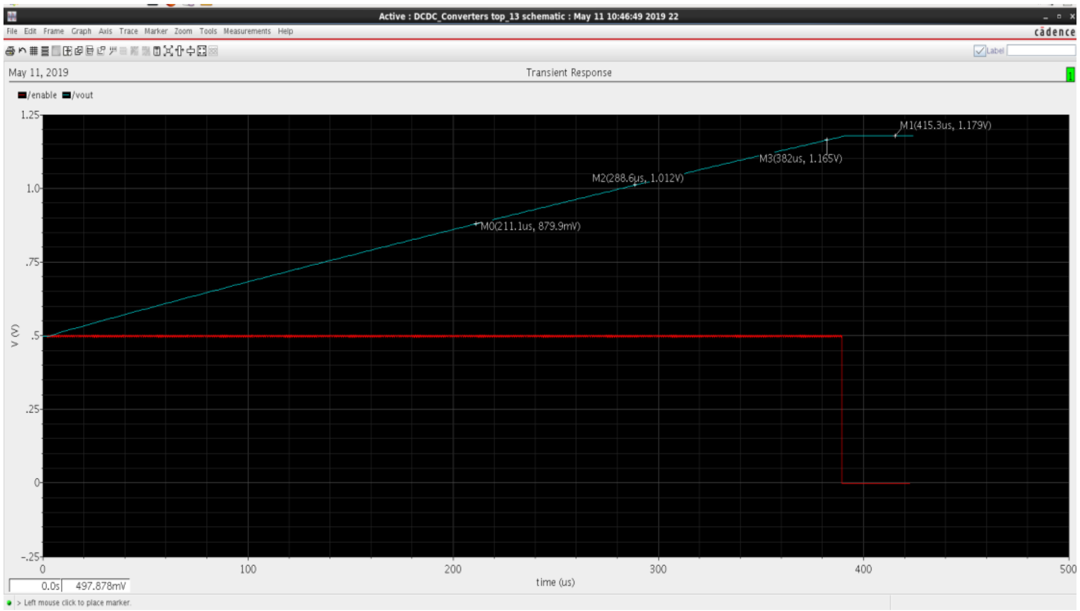

**Fig.6.** Output wave for the integrated inductor less DC-DC converter module for 500mV input voltage.

The transient analysis of integrated Dc-Dc converter is as in figure Fig.6. The Input voltage of 500mV is given to the designed module. And the reference voltage is taken as 1.2 V. The blue line represents the charge pump module output. And red line represents the clock enable. When the output reached 1.179V, the clock generator get disable which in turn stops the charge pump operation. Around 380µSec the charge pump stop pumping and gives the regulated output voltage.

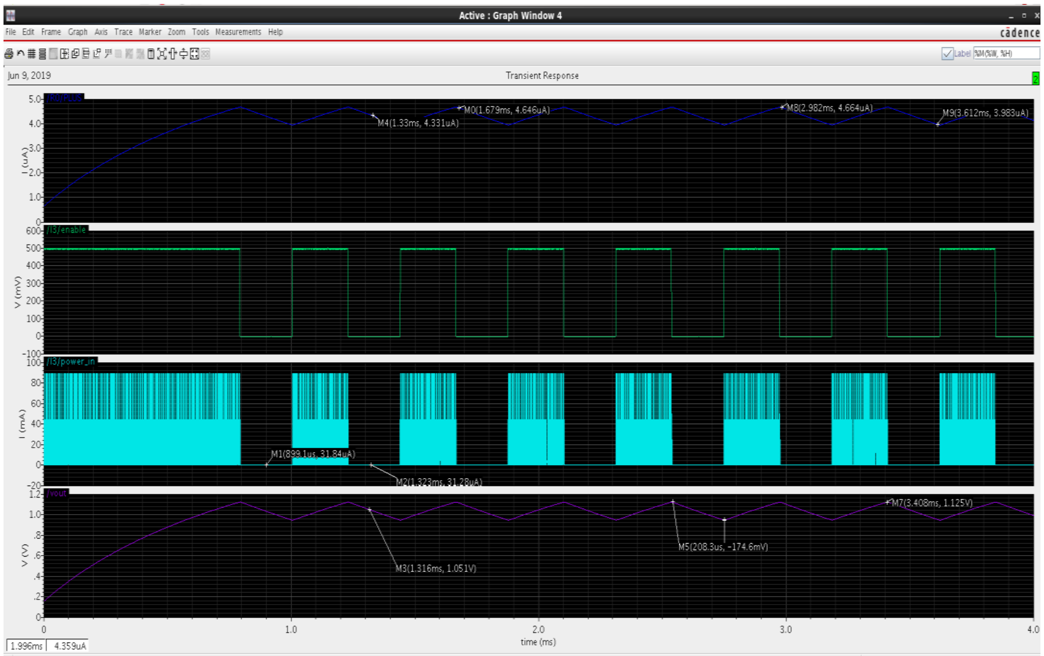

**Fig.7.** Output wave for the integrated inductor less DC-DC converter module for 300mV input voltage

The Fig.7 is the transient output wave form for the integrated module, with the input voltage of 500mV and by taking reference voltage of 800mV then obtained output voltage of 1.125V. In this the output current of 4.67µA and the input current of 31.28µA are shown. Clock enabling and disabling wave form is represented using green line. The power conversion efficiency of 35% is achieved.

TABLE I

Performance summary and comparison table between designed converter and the previous work

| | [6] | [7] | [8] | This work |
|---|---|---|---|---|
| Technology | 130nm | 65nm | 350nm | 45nm |
| External excitation for start up | YES | NO | YES | NO |
| External component | Inductor, Capacitor, MEMS | Inductor, Capacitor | Not needed | Not needed |
| Start voltage | 35mV | 95mV | 500mV | 300mV |
| Regulated output | 1.8V | No | No | 1.2V |
| Regulated efficiency | 30% | n/a | n/a | 35% |

## 5. CONCLUSION

A fully-integrated inductor less Dc-Dc converter provide Regulated Output voltage higher than 1V and the output current up to 5µA starting from around 300mV without using any external excitations. This is implemented in 45nm technology using cadence tool provides the 35% power conversion efficiency. Using this architecture the power consumption and the chip area can be reduced significantly. The converter can be applied for energy harvesting applications such wearable low power electronics circuits and the implantable medical devices.

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